Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: .004” min**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .128” X .160” DATE: 11/9/21**

**MFG: INT’L RECTIFIER THICKNESS .010” P/N: IRFC9140N**

**DG 10.1.2**

#### Rev B, 7/19/02